IEEE 1149.1 Device Architecture
1.1 What Is JTAG?

Joint Test Action Group of IEEE

IEEE Standard 1149.1-1990
“Test Access Port and Boundary-Scan Architecture”

http://standards.ieee.org/catalog

Integrated Circuit Level
Printed Circuit Board Level
Module or System Level

1. IEEE 1149.1 Device Architecture
1.2 Building Blocks of IEEE 1149.1-1990

Any Digital Chip

- Test Data In (TDI)
- Test Clock (TCK)
- Test Mode Select (TMS)
- Test Data Out (TDO)

Each boundary-scan cell can:
- **Capture** data on its parallel input PI
- **Update** data onto its parallel output PO
- **Serially scan** data from SO to its neighbor’s SI
- Behave **transparently**: PI passes to PO
- Note: all digital logic is contained inside the boundary-scan register

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1.3 Providing Boundary-Scan Cells

Question:
How many Boundary-Scan cells per pin are?
Three Boundary-Scan cells per bidirectional pin
(in practice, the two IO scan cells are usually combined into a single multi-function cell BC_7)

Extra Boundary-Scan cell per tristate output pin

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1.4 Boundary-Scan as Internet of Design & Test

**Board Test**
- Prototype Debug (Tektronix)
- In-Circuit Test (Teradyne, HP)
- Functional Test (NI, HP, GenRad)

**System Test**
(Lucent)

**ISP for CPLD**
(Altera, Vantis, Lattice, Xilinx, Cypress, Atmel)

**On-Board Flash Programming**
(Intel, AMD)

**Emulation**
(White Mountain, TI DSP, Lucent DSP)

**Board & IC BIST**
(LogicVision, Mentor)

**Core Chip Test**
(LogicVision, Mentor)

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1.5 IEEE 1149.1 Device Architecture

**TDI:** Serial data in sampled on rising edge default = 1

**TDO:** Serial data out sampled on failing edge default = Z

**TMS:** Input control sampled on rising edge default = 1

**TCK:** Dedicated clock any frequency

**TRST**: Optional async reset active low default = 1
1.6 The Instruction Set

**Mandatory instructions** *(since 1149.1-2001)*

- **BYPASS**: Insert one-bit register to reduce serial path length
- **SAMPLE**: Take snapshot of current data
- **PRELOAD**: Take snapshot of current data
- **EXTEST**: Test external connections

**Optional instructions**

- **IDCODE**: Insert ID register into scan chain
- **INTEST**: Test internal circuitry
- **CLAMP**: Scan cell data to outputs, insert Bypass register
- **HIGHZ**: Outputs high-Z state, insert Bypass register
- **RUNBIST**: Starts the Built-In-Self-Test for the device

NOTE: All unused instruction codes must default to **BYPASS**

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1.7 Using the Instruction Register

**Problem:** Set device 1 in *BYPASS*, devices 2 & 3 in *EXTEST* ready for interconnect test.

**Step 1:** Select IRs as active registers in all devices.
Load *BYPASS* code into 1 (all-1s), *EXTEST* code into 2 & 3 (all-0s)

**Step 2:** Decode and execute new instructions. New target registers are selected

**Step 3:** Devices now set up to apply interconnect tests between devices 2 & 3

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