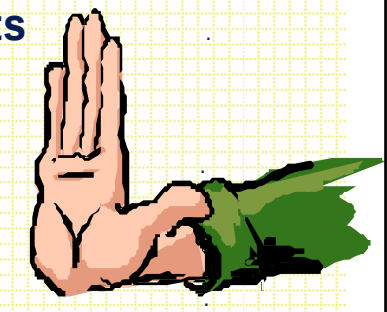
DFT Checklist – *DO !*

- Maximize controllability & observability using logical or physical points
- Partition large circuits into smaller sub-circuits to ease pattern generation
- Avoid the use of redundant logic
- Avoid wired logic configurations
- Avoid ground bounce
- Be conservative on fan-out to accommodate probe loading
- Simple sets, resets and control lines
- Keep analogue and digital circuits apart for separate test techniques
- Buffer edge-sensitive signals, e.g. ECL to TTL/CMOS levels
- Tie off unused inputs rather than leave them floating
- Shorten counters and shift registers by using a free input pin to divide long counters in half
- Plan trade-offs for ICT pads placing
- Use Boundary-Scan as much as possible
- Understand the limits of the target tester
- Provide adequate documentation from design to test

DFT Checklist – *DON'T !*

- Use asynchronous logic (unpredictable behavior when faulty)
- Use monostables/one-shots (uncontrollable behavior under test conditions)
- Make use of redundancy without providing access to redundant nets
- Use a mix of technologies on a board: difficult to separate and test
- Allow floating nodes: tie them off
- Coat a board with conformal coating before ICT
- Use non-compliant Boundary-Scan devices



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Explanations and details ?

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