SVF and JAM files creation rules for the CPLD In-System Programming and the FPGA In-System Configuration with JTAG test stations

Rules for R&D labs to facilitate our teamwork

Altera CPLD & FPGA devices

1. Launch Altera **Quartus II**

2. Go to ***Tools\Programmer*** in the upper menu

3. In the right vertical menu go to ***Add File …*** and select the appropriate programming file (for example, ***.pof** for CPLD or ***.jic** for FPGA)

4. In the upper menu go to
   File…Create /Update … Create JAM, SVF, or ISC File … and click it

5. Select File name as you wish.
   Select File format as Serial Vector Format (**SVF**) for CPLD or
   as **JAM** for FPGA

   (Attention: make **JAM** file from **JIC** only, NOT from ***.pof** or ***.sof** !)

   Select Operation - Program
   Leave Blank-check window empty
   All another windows here are don't care

6. If the Altera device programming is intended to be via Corelis TAP1 only, change the SVF file name to the following one:

   <file name>_Altera.svf (or <file name>_Altera.jam)

7. If the Altera device programming is intended to do via Corelis TAP1 and

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TAP2 and the *.pof is made for two TAPs, change the SVF file name to the following one:

<file name>_tap1+2_Altera.svf
(or **<file name>_Altera_tap1+2.jam)**

8. If the Altera device programming is intended to do via Corelis TAP1, TAP2, TAP3, and the *.pof is made for three TAPs, change the SVF file name to the following one:

<file name>_tap1+2+3_Altera.svf
(or **<file name>_Altera_tap1+2+3.jam)**

9. Launch your Corelis test plan (*.tsp file).
Click Setup/Test Plan (or simple F2), then Add, and insert the ***_Altera.svf** file (or the ***_Altera.jam** file) to the appropriate place in the test plan.

10. Right click on the name of the ***_Altera.svf** (or the ***_Altera.jam** file) into the test plan, click ***Options***. Check the "Use the Following Chain Position" and select the Reference Name of the Altera device (CPLD or FPGA) you will to program with this file.

11. All another options (for the **SFV** format) leave as before.

12. For the **JAM** format check the "***Other Action***" and insert the word "**Configure**" in the corresponding window for both Erase and Program actions.

WARNING: the FPGA's BSDL file alters after the FPGA configuration !!!

13. Save the test plan.

14. Your CPLD programming step (or FPGA configuration stap) in the Corelis test program is ready to use.

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Lattice CPLD devices

1. Launch Lattice **ispVM System**

2. Click ***File\New*** in the upper menu

3. Click **Add Device(Ins)** in the upper menu

4. Fill the Device Information window:

   - Part description – according to your schematics
   - Select Device – according to Device Family, Device Name & Package
   - Data File – browse your CPLD configuration file in the *.jed format
   - Operation – select the operation mode you prefer, for example, “Erase, Program, Verify” or “Erase only”
   - Click OK

5. Click **SVF** in the upper menu. In the Generate SVF File window select option “Build SVF File for Single Device. In “Data File” – browse your CPLD configuration file in the *.jed format

6. Change the SVF file name in the “Save SVF File as …” window to the following one

   <file name>_Program_Lattice.svf if the file is intended for programming

   or to the

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<file name>_Erase_Lattice.svf svf if the file is intended for erasing via Corelis TAP1 only.

Change these names to ***<file name>_Program_tap1+2_Lattice.svf*** or to the ***<file name>_Erase_tap1+2_Lattice.svf*** if you're working via Corelis TAP1 and TAP2, etc.

7. Click **Generate.**

8. Launch your Corelis test plan (*.tsp file).

   Click Setup/Test Plan (or simple F2), then Add, and insert the **<file name>_Lattice.svf** file to the appropriate place into the test plan.

9. Right click on the name of the **<file name>_ Lattice.svf** in the test plan, click Options.

10. Check the "Use the Following Chain Position" and select the reference name of the Lattice device you will to program with this file.

11. All another options leave as before. Save the test plan.

12. Your CPLD programming step in the Corelis test program is now ready to use.

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<u>Xilinx CPLD & FPGA devices</u>

1. Download from the Xilinx website the free copy or the most recent version of the **iMPACT** software (the Xilinx WebPACK area)

   The following description is based on the iMPACT Release 10.1

2. Launch Xilinx **iMPACT**

3. Left double click on **Boundary Scan** in the <u>Flows</u> window

4. Right click in the workspace to add the Xilinx device *.jed configuration file via browser.

5. Add into the JTAG chain you got all additional JTAG devices that are physically connected into the chain (according to their order and places) by selection of their BSDL files.

6. Right click in the workspace and select:

   Output File Type / SVF File / Create SVF File ...

7. Select the name & destination of the new SVF file via browser. The SVF file name structure for the Corelis JTAG station usage must to be as following:
   <file name>_Xilinx.svf

   if you're working via Corelis TAP1 only.

   Change this name to ***<file name>_tap1+2_ Xilinx.svf*** if you're working via Corelis TAP1 and TAP2, etc.

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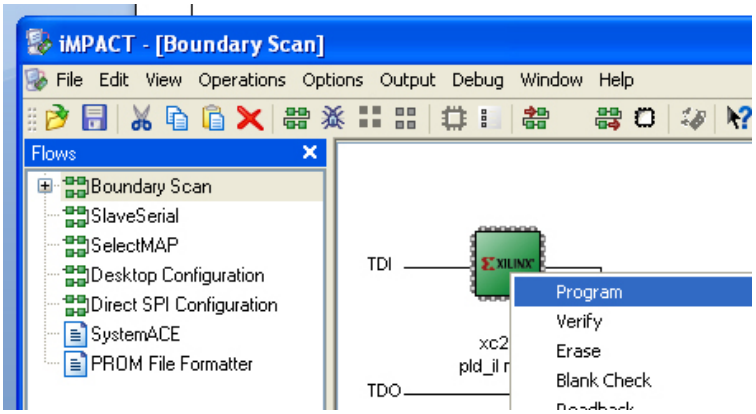
The workspace is now in the **SVF File Mode** – see upper right corner.

8. Right click on the GREY picture of the device intended for configuration (became GREEN) to select the required operation of the SVF file – **Program**, **Verify**, or **Erase**.



9. Pay attention on the result message at the bottom, for example:

10. Left click then right click in the workspace and select:

Output File Type / SVF File / Stop Writing to File